WHAT IS CLAIMED IS:

1. A disk array control apparatus comprising a plurality of disk array control units, each having:

a channel interface interfacing with a host computer;

a disk interface interfacing with a magnetic disk device;

a cache memory for temporarily storing data to be read/written from/to the magnetic disk device;

a shared memory portion for storing control information concerning data transfer between the channel interface and the cache memory and between the disk interface and the cache memory and management information of the magnetic disk device;

connection means (thick line) for connecting the channel interface and the disk interface to the cache memory; and

connection means (thick line) for connecting the channel interface and the disk interface to the shared memory portion;

wherein for data read/write request from the host computer, the channel interface performs data transfer between the interface with the host computer and the cache memory while the disk interface performs data transfer between the magnetic disk device and the cache memory, thereby performing data read/write, and

wherein connection network means is provided for connection between the shared memory portions in

the plurality of disk array control units and connection network means is provided for connection between the cache memories in the plurality of disk array control units, thereby enabling transfer processing requiring data transfer between the shared memory portion in one of the disk array control units and the shared memory portion in another disk array control unit.

2. A disk array control apparatus comprising a plurality of disk array control units, each having:

a channel interface interfacing with a host computer;

a disk interface interfacing with a magnetic disk device;

a cache memory for temporarily storing data to be read/written from/to the magnetic disk device;

a shared memory portion for storing control information concerning data transfer between the channel interface and the cache memory and between the disk interface and the cache memory and management information of the magnetic disk device;

connection means (thick line) for connecting the channel interface and the disk interface to the cache memory; and

connection means (thick line) for connecting the channel interface and the disk interface to the shared memory portion;

wherein for data read/write request from the

host computer, the channel interface performs data transfer between the interface with the host computer and the cache memory while the disk interface performs data transfer between the magnetic disk device and the cache memory, thereby performing data read/write, and

wherein connection network means is provided for connection between the shared memory portions in the plurality of disk array control units and connection network means is provided for connection between the cache memories in the plurality of disk array control units, thereby enabling transfer processing requiring data transfer between the shared memory portion in one of the disk array control units and the shared memory portion in another disk array control unit as well as data read/write processing to a transfer processing domain from the channel interface and the disk interface in the disk array control unit even during a transfer processing.

3. The disk array control apparatus as claimed in Claim 1, wherein the plurality of channel interfaces and the plurality of disk interfaces are connected to the plurality of cache memories by an interconnection network using a switch capable of being switched to the plurality of disk array control units; and the plurality of channel interfaces and the plurality of disk interfaces are connected to the plurality of shared memory portions by an interconnection network using a switch capable of being switched to the

plurality of disk array control units; thereby enabling to perform a transfer processing requiring data transfer between the shared memory portions in one of the disk array control units and the shared memory portion in another disk array control units.

4. The disk array control apparatus as claimed in Claim 1, wherein the interconnection network is used for data transfer from the shared memory portion in one of the disk array control units to the shared memory portion in another disk array control unit and recording means is provided for indicating which domain of she shared memory in the shared memory portion has completed transfer.

5. The disk array control apparatus as claimed in Claim 1, wherein the interconnection network is used for data transfer from the shared memory portion in one of the disk array control units to the shared memory portion in another disk array control unit and monitor information is provided for monitoring frequency in use of the interconnection network so that data transfer is performed when the frequency in use of the interconnection network is low.

6. The disk array control apparatus as claimed in Claim 1, wherein the interconnection network is used for data transfer from the shared memory portion in one of the disk array control units to the shared memory portion in another disk array control unit,

when a read request is made, during a data

transfer, to the shared memory portion of the transfer destination, it is determined whether the shared memory of the shared memory portion is a transfer end domain and if the shared memory is the transfer end domain, then data is read out from the shared memory of the transfer destination shared memory portion and if the shared memory is a transfer non-end domain, data is read out from the shared memory of the transfer source shared memory portion, and

when a write request is made, during data transfer, to the shared memory of the shared memory portion of the transfer destination, data is written into the shared memory of the transfer destination shared memory portion and the corresponding shared memory domain of the transfer source shared memory portion, enabling to asynchronously perform data transfer without affecting other data processing which is transferring data.

7. The disk array control apparatus as claimed in Claim 1, wherein the interconnection network is used for data transfer from the shared memory portion in one of the disk array control units to the shared memory portion in another disk array control unit, and during a data transfer, a micro-program of the channel interface or the disk interface can perform read/write processing without considering that the transfer processing is in progress.

8. The disk array control apparatus as claimed

in Claim 1, wherein the shared memory portion in the disk array control unit has a reserved domain not used for normal operation and the interconnection network is used for transferring data from the shared memory portion in the disk array control unit to the reserved domain of the shared memory portion in another disk array control unit.

9. The disk array control apparatus as claimed in Claim 1, wherein connection network means is provided for connecting the disk interface and the channel interfaces in the plurality of disk array control units and the connection network means is connected to a service processor managing configuration information of the disk array control apparatus, so that the service processor can perform addition/removal and moving of a disk, a logic volume, a disk control device, and the like, thereby enabling to control the plurality disk array control units by the single service processor.

10. The disk array control apparatus as claimed in Claim 1, wherein the shared memory portion includes transfer control means for setting transfer control information for data transfer; the transfer control means includes: transfer source start address means where a transfer source start address of the shared memory of the data transfer source is loaded, transfer execution bit means where a valid bit indicating a data transfer start is loaded, address generation logic

means which is executed when a valid bit is set in the transfer execution bit means, transfer decision logic means, and transfer end decision logic means.

11. The disk array control apparatus as claimed in Claim 10, the apparatus further comprising transfer execution address unit where a transfer execution address is set during a data transfer and a counter which is increment each time a data transfer request is made from a data transfer source.

12. A control data transfer method of using a plurality of disk array control means for controlling data transfer between a plurality of host computers and a plurality of magnetic disk devices via channel interface and disk interface when control information concerning data transfer between the host computers and cache memories and management information of the magnetic disk devices are transferred from one of the disk array control means to another of the disk array control means, the method comprising the steps of:

(a) instructing a data transfer request from a micro-program of the channel interface of a data transfer source to the shared memory portion of the disk array control means;

(b) setting a transfer source start address of the shared memory of the data transfer source in transfer source start address means of a data transfer destination;

(c) setting a transfer destination start address

of the shared memory of the data transfer destination in the transfer destination start address means;

(d) setting a transfer end address of the shared memory of the data transfer destination in transfer destination end address means;

(e) setting a valid bit indicating a data transfer start in transfer execution bit means of the transfer destination:; and

(f) performing data transfer by setting the valid bit to execute address generation logic means for data transfer, transfer decision logic means for deciding a state of the data transfer, and transfer end decision logic means.